IN THE CLAIMS

1-42. (Canceled)

43. (Original) An input buffer protection circuit comprising:

an input node to receive an input signal;

an internal signal node coupled to communicate the input signal to an input buffer circuit;

a pass transistor coupled between the input node and the internal signal node;

a bias circuit coupled to the internal signal node, wherein the bias circuit and the pass transistor are coupled to be controlled by an inhibitor signal such that the bias circuit is active to bias the internal signal node to a predetermined voltage while the pass transistor is deactivated to interrupt a signal path from the input node to the internal signal node; and

control circuitry to provide the inhibitor signal.

44. (Original) The input buffer protection circuit of claim 43 wherein the control circuitry comprises transistors to deactivate the pass transistor and to activate the bias circuit when the input signal reaches a predetermined threshold voltage level.

45. (Original) The input buffer protection circuit of claim 43 wherein:

the pass transistor comprises an n-channel transistor comprising a gate coupled to receive the inhibitor signal, a drain, and a source; and

the bias circuit comprises a pair of p-channel transistors and a resistor coupled in series between a voltage supply and the internal signal node, gates of each of the pair of p-channel transistors being coupled to receive the inhibitor signal.

46. (Original) The input buffer protection circuit of claim 43 wherein the control circuitry comprises:

a voltage sensor coupled to receive a pumped signal and the input signal, the voltage sensor to generate a sensed signal in response to the pumped signal and the input signal; and

an inhibiting circuit coupled to receive the pumped signal and coupled to the voltage

sensor to receive the sensed signal, the inhibiting circuit being coupled to the pass transistor to generate the inhibitor signal in response to the pumped signal and the sensed signal.

47. (Original) An integrated circuit comprising:

an input node to receive an input signal;

an internal signal node coupled to communicate the input signal to an input buffer circuit;

a pass transistor coupled between the input node and the internal signal node;

a bias circuit coupled to the internal signal node, wherein the bias circuit and the pass transistor are coupled to be controlled by an inhibitor signal such that the bias circuit is active to bias the internal signal node to a predetermined voltage while the pass transistor is deactivated to interrupt a signal path from the input node to the internal signal node; and

control circuitry to provide the inhibitor signal to activate the pass transistor and deactivate the bias circuit while the input signal is less than a predetermined threshold voltage level, and to deactivate the pass transistor and activate the bias circuit when the input signal reaches the predetermined threshold voltage level.

48. (Original) The integrated circuit of claim 47 wherein:

the pass transistor comprises an n-channel transistor comprising a gate coupled to receive the inhibitor signal, a drain, and a source; and

the bias circuit comprises a pair of p-channel transistors and a resistor coupled in series between a voltage supply and the internal signal node, gates of each of the pair of p-channel transistors being coupled to receive the inhibitor signal.

49. (Original) The integrated circuit of claim 47 wherein the control circuitry comprises:

a voltage sensor coupled to receive a pumped signal and the input signal, the voltage sensor to generate a sensed signal in response to the pumped signal and the input signal; and

an inhibiting circuit coupled to receive the pumped signal and coupled to the voltage sensor to receive the sensed signal, the inhibiting circuit being coupled to the pass transistor to generate the inhibitor signal in response to the pumped signal and the sensed signal.

50. (Original) A memory device comprising:

an input node to receive an input signal;

an internal signal node coupled to communicate the input signal to an input buffer circuit;

a pass transistor coupled between the input node and the internal signal node;

a bias circuit coupled to the internal signal node, wherein the bias circuit and the pass transistor are coupled to be controlled by an inhibitor signal such that the bias circuit is active to bias the internal signal node to a predetermined voltage while the pass transistor is deactivated to interrupt a signal path from the input node to the internal signal node; and

control circuitry to provide the inhibitor signal to activate the pass transistor and deactivate the bias circuit while the memory device is in a non-test operation, and to deactivate the pass transistor and activate the bias circuit when the memory device is in a test mode indicated by an elevated voltage greater than a predetermined threshold voltage level provided on the input node.

51. (Original) The memory device of claim 50 wherein:

the pass transistor comprises an n-channel transistor comprising a gate coupled to receive the inhibitor signal, a drain, and a source; and

the bias circuit comprises a pair of p-channel transistors and a resistor coupled in series between a voltage supply and the internal signal node, gates of each of the pair of p-channel transistors being coupled to receive the inhibitor signal.

52. (Original) The memory device of claim 50 wherein the control circuitry comprises:

a voltage sensor coupled to receive a pumped signal and the input signal, the voltage sensor to generate a sensed signal in response to the pumped signal and the input signal; and

an inhibiting circuit coupled to receive the pumped signal and coupled to the voltage sensor to receive the sensed signal, the inhibiting circuit being coupled to the pass transistor to generate the inhibitor signal in response to the pumped signal and the sensed signal.

53. (Original) A method of operating an input buffer comprising:

receiving an input signal at an input node;

communicating the input signal to an input buffer circuit through an internal signal node;

controlling a pass transistor coupled between the input node and the internal signal node and a bias circuit coupled to the internal signal node with an inhibitor signal to activate the bias circuit to bias the internal signal node to a predetermined voltage while the pass transistor is deactivated to interrupt a signal path from the input node to the internal signal node; and

providing the inhibitor signal from control circuitry.

54. (Original) The method of claim 53 wherein controlling a pass transistor and a bias circuit further comprises deactivating the pass transistor and activating the bias circuit when the input signal reaches a predetermined threshold voltage level.

55. (Original) The method of claim 53 wherein:

controlling a pass transistor further comprises controlling an n-channel transistor comprising a gate, a drain, and a source by coupling the inhibitor signal to the gate of the n-channel transistor; and

controlling a bias circuit further comprises controlling a pair of p-channel transistors and a resistor coupled in series between a voltage supply and the internal signal node by coupling the inhibitor signal to gates of each of the pair of p-channel transistors.

56. (Original) The method of claim 53 wherein providing the inhibitor signal further comprises:

receiving a pumped signal and the input signal in a voltage sensor, and generating a sensed signal in the voltage sensor in response to the pumped signal and the input signal; and

receiving the pumped signal and the sensed signal in an inhibiting circuit, and generating the inhibitor signal in the inhibiting circuit in response to the pumped signal and the sensed signal.

57. (Original) A method of operating an integrated circuit comprising:

receiving an input signal at an input node;

communicating the input signal to an input buffer circuit through an internal signal node;

controlling a pass transistor coupled between the input node and the internal signal node and a bias circuit coupled to the internal signal node with an inhibitor signal to activate the bias circuit to bias the internal signal node to a predetermined voltage while the pass transistor is deactivated to interrupt a signal path from the input node to the internal signal node; and

providing the inhibitor signal from control circuitry to activate the pass transistor and deactivate the bias circuit while the input signal is less than a predetermined threshold voltage level, and to deactivate the pass transistor and activate the bias circuit when the input signal reaches the predetermined threshold voltage level.

58. (Original) The method of claim 57 wherein:

controlling a pass transistor further comprises controlling an n-channel transistor comprising a gate, a drain, and a source by coupling the inhibitor signal to the gate of the n-channel transistor; and

controlling a bias circuit further comprises controlling a pair of p-channel transistors and a resistor coupled in series between a voltage supply and the internal signal node by coupling the inhibitor signal to gates of each of the pair of p-channel transistors.

59. (Original) The method of claim 57 wherein providing the inhibitor signal further comprises:

receiving a pumped signal and the input signal in a voltage sensor, and generating a sensed signal in the voltage sensor in response to the pumped signal and the input signal; and

receiving the pumped signal and the sensed signal in an inhibiting circuit, and generating the inhibitor signal in the inhibiting circuit in response to the pumped signal and the sensed signal.

60. (Original) A method of operating a memory device comprising:

receiving an input signal at an input node;

communicating the input signal to an input buffer circuit through an internal signal node;

controlling a pass transistor coupled between the input node and the internal signal node and a bias circuit coupled to the internal signal node with an inhibitor signal to activate the bias

circuit to bias the internal signal node to a predetermined voltage while the pass transistor is deactivated to interrupt a signal path from the input node to the internal signal node; and

providing the inhibitor signal from control circuitry to activate the pass transistor and deactivate the bias circuit while the memory device is in a non-test operation, and to deactivate the pass transistor and activate the bias circuit when the memory device is in a test mode indicated by an elevated voltage greater than a predetermined threshold voltage level provided on the input node.

61. (Original) The method of claim 60 wherein:

controlling a pass transistor further comprises controlling an n-channel transistor comprising a gate, a drain, and a source by coupling the inhibitor signal to the gate of the n-channel transistor; and

controlling a bias circuit further comprises controlling a pair of p-channel transistors and a resistor coupled in series between a voltage supply and the internal signal node by coupling the inhibitor signal to gates of each of the pair of p-channel transistors.

62. (Original) The method of claim 60 wherein providing the inhibitor signal further comprises:

receiving a pumped signal and the input signal in a voltage sensor, and generating a sensed signal in the voltage sensor in response to the pumped signal and the input signal; and

receiving the pumped signal and the sensed signal in an inhibiting circuit, and generating the inhibitor signal in the inhibiting circuit in response to the pumped signal and the sensed signal.

63. (Original) An input system for a low-voltage flash memory device, comprising:

an input buffer comprising:

an input stage comprising a transistor comprising a gate, a drain, and a source, the gate being coupled to receive an inhibiting signal and the drain being coupled to receive an input signal, the transistor being controlled to inhibit the input signal from being presented at the source when the inhibiting signal is at a first predetermined level; and

an output stage coupled to the input stage to present the input signal to the low-voltage flash memory device; and

a voltage sensor coupled to receive the input signal and a pumped signal to trigger when the input signal is at a second predetermined level.

64. (Original) The input system of claim 63 wherein:

the transistor comprises an n-channel transistor; and

the output stage comprises an inverter comprising a first connection and a second connection, the first connection being coupled to the source of the transistor and the second connection to present the input signal to the low-voltage flash memory device.

65. (Original) The input system of claim 63 wherein the voltage sensor comprises a triggering stage comprising a set of p-channel transistors and a set of n-channel transistors coupled to receive to the input signal.

66. (Original) The input system of claim 65 wherein the voltage sensor further comprises:

a set of metal options;

an inverting stage; and

a delay stage to reject undesired noise.

67. (Original) The input system of claim 63, further comprising an inhibiting circuit coupled to receive the pumped signal and coupled to the voltage sensor to receive a sensed signal generated by the voltage sensor, the inhibiting circuit being coupled to the input buffer to generate the inhibiting signal in response to the pumped signal and the sensed signal.

68. (Original) An input system for a low-voltage flash memory device, comprising:

an input buffer comprising:

an input stage comprising a transistor comprising a gate, a drain, and a source, the gate being coupled to receive an inhibiting signal and the drain being coupled to receive an input signal, the transistor being controlled to inhibit the input signal from being presented at the

source when the inhibiting signal is at a first predetermined level; and

an output stage coupled to the input stage to present the input signal to the low-voltage flash memory device; and

an inhibiting circuit coupled to the input buffer to selectively produce the inhibiting signal, the inhibiting circuit being coupled to receive a pumped signal and a sensed signal.

69. (Original) The input system of claim 68 wherein:

the transistor comprises an n-channel transistor; and

the output stage comprises an inverter comprising a first connection and a second connection, the first connection being coupled to the source of the transistor and the second connection to present the input signal to the low-voltage flash memory device.

70. (Original) The input system of claim 68, wherein the inhibiting circuit comprises:

a first n-channel transistor comprising a gate coupled to receive the sensed signal, a drain coupled to present the inhibiting signal, and a source coupled to ground;

a second n-channel transistor comprising a gate coupled to an inverted sensed signal, a drain, and a source coupled to ground;

a first p-channel transistor comprising a gate coupled to the drain of the second n-channel transistor, a drain coupled to the drain of the first n-channel transistor, a source coupled to receive the pumped signal, and a bias coupled to receive the pumped signal; and

a second p-channel transistor comprising a gate coupled to the drain of the first n-channel transistor, a drain coupled to the drain of the second n-channel transistor, a source coupled to receive to the pumped signal, and a bias coupled to receive the pumped signal.

71. (Original) The input system of claim 26, further comprising a voltage sensor coupled to receive the pumped signal and the input signal, the voltage sensor to generate the sensed signal, the inhibiting circuit being coupled to the voltage sensor to generate the inhibiting signal in response to the pumped signal and the sensed signal.

Claims 1-42 have been canceled, claims 43-71 are therefore pending in this application. The Examiner is invited to contact the below-signed attorney with any questions regarding the present application.

Respectfully Submitted,

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